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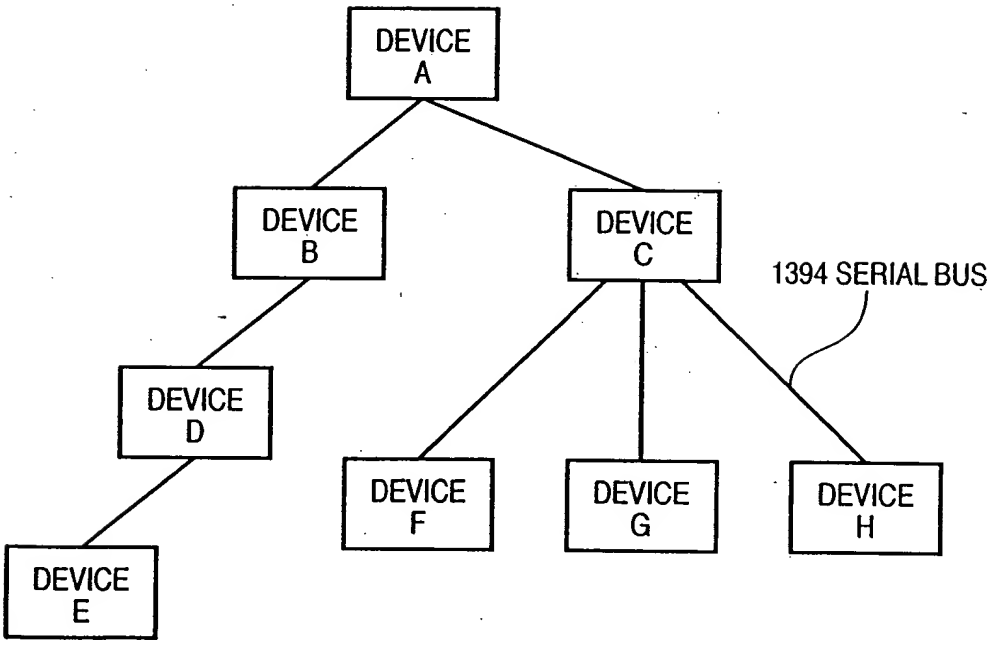
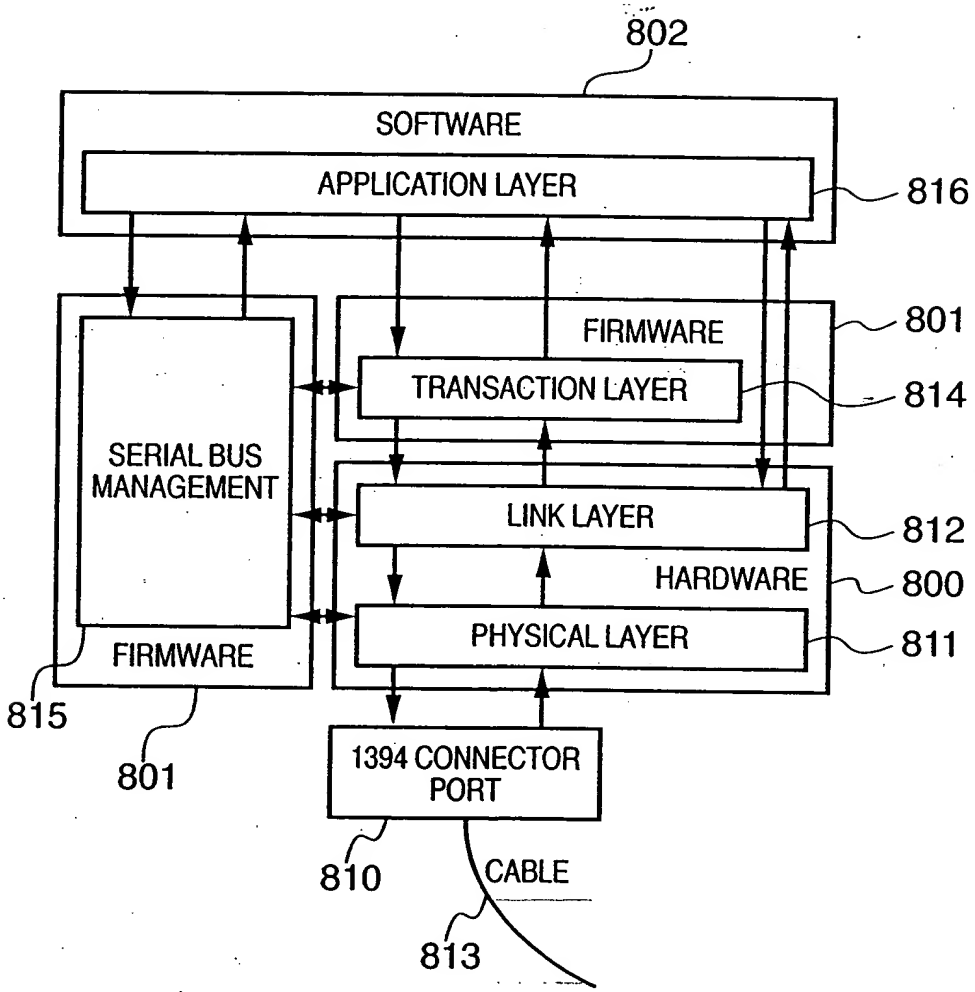
FIG. 1



# FIG. 2


802
SOFTWARE
APPLICATION LAYER
816
FIRMWARE
801
TRANSACTION LAYER
814
SERIAL BUS MANAGEMENT
LINK LAYER
812
HARDWARE
800
PHYSICAL LAYER
811
FIRMWARE
815
801
1394 CONNECTOR PORT
810
CABLE
813

# FIG. 3

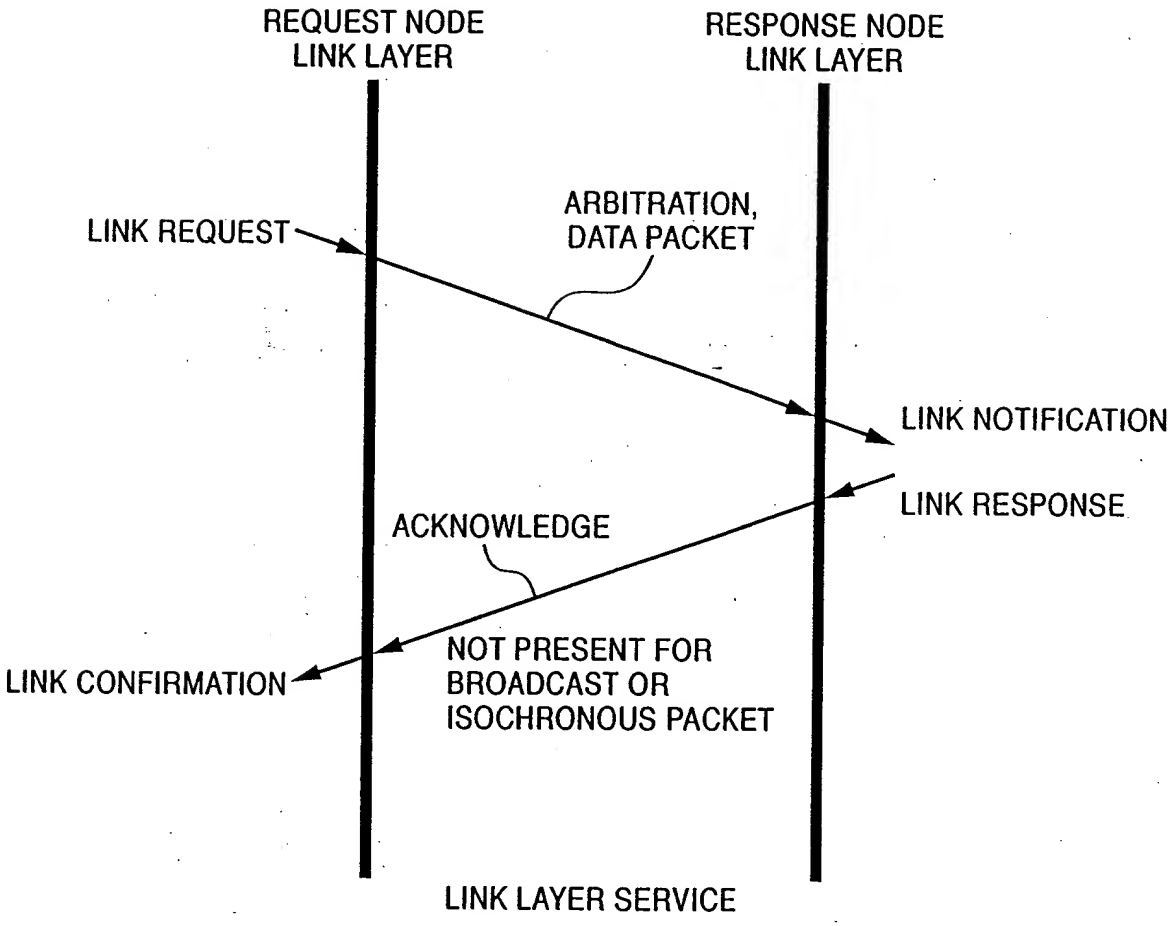



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FIG. 4

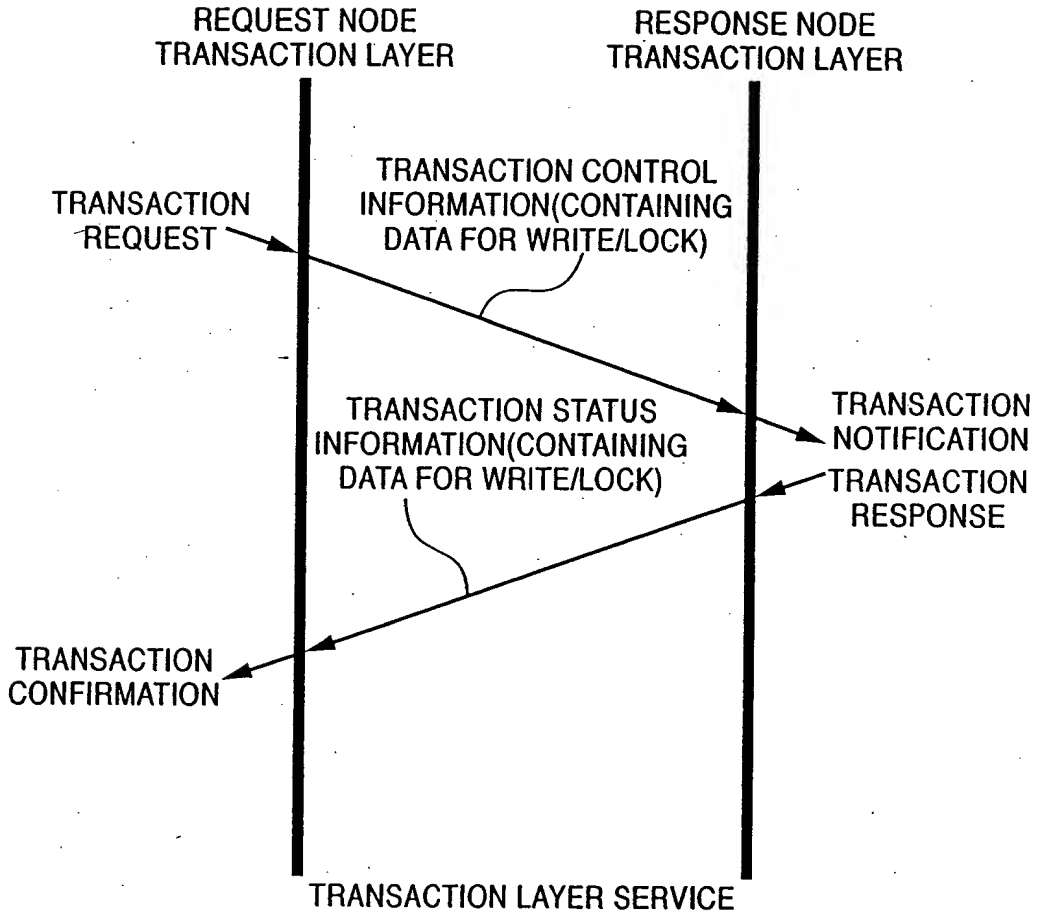
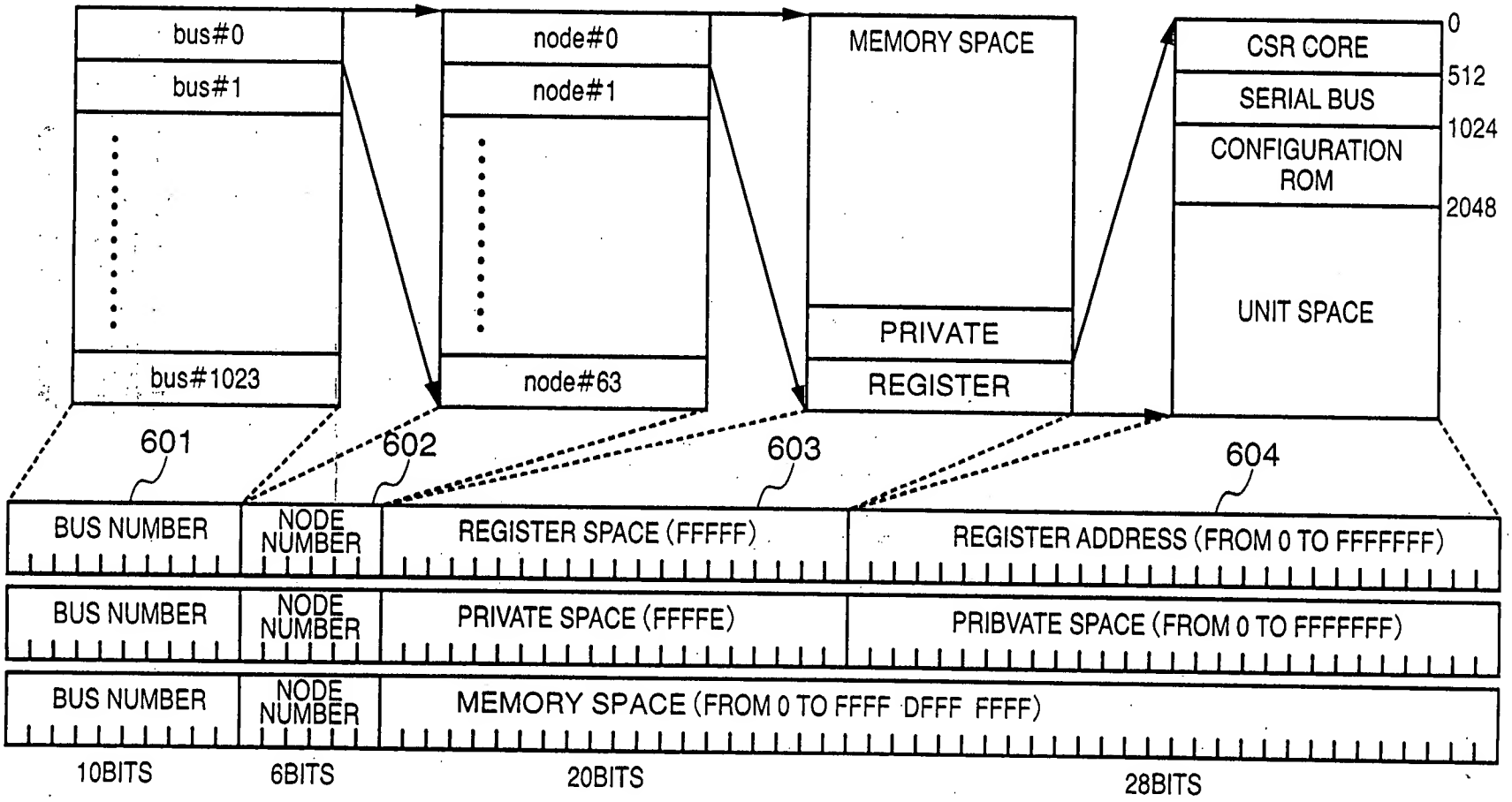

REQUEST NODE
TRANSACTION LAYER
RESPONSE NODE
TRANSACTION LAYER
TRANSACTION
REQUEST
TRANSACTION CONTROL
INFORMATION(CONTAINING
DATA FOR WRITE/LOCK)
TRANSACTION
NOTIFICATION
TRANSACTION STATUS
INFORMATION(CONTAINING
DATA FOR WRITE/LOCK)
TRANSACTION
RESPONSE
TRANSACTION
CONFIRMATION
TRANSACTION LAYER SERVICE

FIG. 5


bus#0
bus#1
bus#1023
node#0
node#1
node#63
MEMORY SPACE
PRIVATE
REGISTER
CSR CORE
SERIAL BUS
CONFIGURATION ROM
UNIT SPACE
0
512
1024
2048
601
602
603
604
BUS NUMBER
NODE NUMBER
REGISTER SPACE (FFFFF)
REGISTER ADDRESS (FROM 0 TO FFFFFFF)
BUS NUMBER
NODE NUMBER
PRIVATE SPACE (FFFFE)
PRIBVATE SPACE (FROM 0 TO FFFFFFF)
BUS NUMBER
NODE NUMBER
MEMORY SPACE (FROM 0 TO FFFF DFFF FFFF)
10BITS
6BITS
20BITS
28BITS

# FIG. 6

| CSR CORE REGISTER | | |
|---|---|---|
| OFFSET (HEXADECIMAL) | REGISTER NAME | FUNCTION |
| 000 | STATE_CLEAR | STATE AND CONTROL INFORMATION |
| 004 | STATE_SET | INFORMATION REPRESENTING STATE_CLEAR WRITE |
| 008 | NODE_IDS | BUS ID + NODE ID |
| 00C | RESET_START | BUS IS RESET BY WRITE IN THIS AREA |
| 010~014 | INDIRECT_ADDRESS, INDIRECT_DATA | REGISTER FOR ACCESSING FOR LARGER THAN 1K |
| 018~01C | SPLIT_TIMEOUT | VALUE OF TIMER FOR DETECTING TIMEOUT OF SPLIT TRANSACTION |
| 020~02C | ARGUMENT, TEST_START, TEST_STATUS | REGISTER FOR DIAGNOSIS |
| 030~04C | UNITS_BASE, UNITS_BOUND, MEMORY_BASE, MEMORY_BOUND | NOT PREPARED FOR IEEE1394 |
| 050~054 | INTERRUPT_TARGET, INTERRUPT_MASK | INTERRUPT NOTIFICATION REGISTER |
| 058~07C | CLOCK_VALUE, CLOCK_TICK_PERIOD, CLOCK_STOROBE_ARRIVED, CLOCK_INFO | NOT PREPARED FOR IEEE1394 |
| 080~0FC | MESSAGE_REQUEST, MESSAGE_RESPONSE | MESSAGE NOTIFICATION REGISTER |
| 100~17C | | RESERVATION |
| 180~1FC | ERROR_LOG_BUFFER | RESERVATION FOR IEEE1394 |

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# FIG. 7

| SERIAL BUS REGISTER | | |
|---|---|---|
| OFFSET (HEXADECIMAL) | REGISTER NAME | FUNCTION |
| 200 | CYCLE_TIME | COUNTER FOR ISOCHRONOUS TRANSFER |
| 204 | BUS_TIME | REGISTER FOR TIME SYNCHRONIZATION |
| 208 | POWER_FAIL_IMMINENT | REGISTER RELATED TO POWER SUPPLY |
| 20C | POWER_SOURCE | |
| 210 | BUSY_TIMEOUT | CONTROLLING RETRY OF TRANSACTION LAYER |
| 214 ~ 218 | | RESERVATION |
| 21C | BUS_MANAGER_ID | NODE ID OF BUS MANAGER |
| 220 | BANDWIDTH_AVAILABLE | MANAGING BAND FOR ISOCHRONOUS TRANSFER |
| 224 ~ 228 | CHANNELS_AVAILABLE | MANAGING CHANNEL NUMBER OF ISOCHRONOUS TRANSFER |
| 22C | MAINT_CONTROL | REGISTER FOR DIAGNOSIS |
| 230 | MAINT_UTILITY | |
| 234 ~ 3FC | | RESERVATION |

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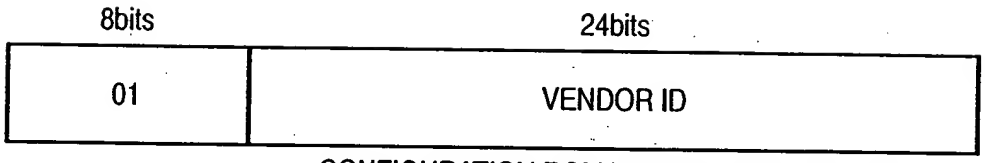
FIG. 8




CONFIGURATION ROM WITH MINIMAL FORMAT

# FIG. 9

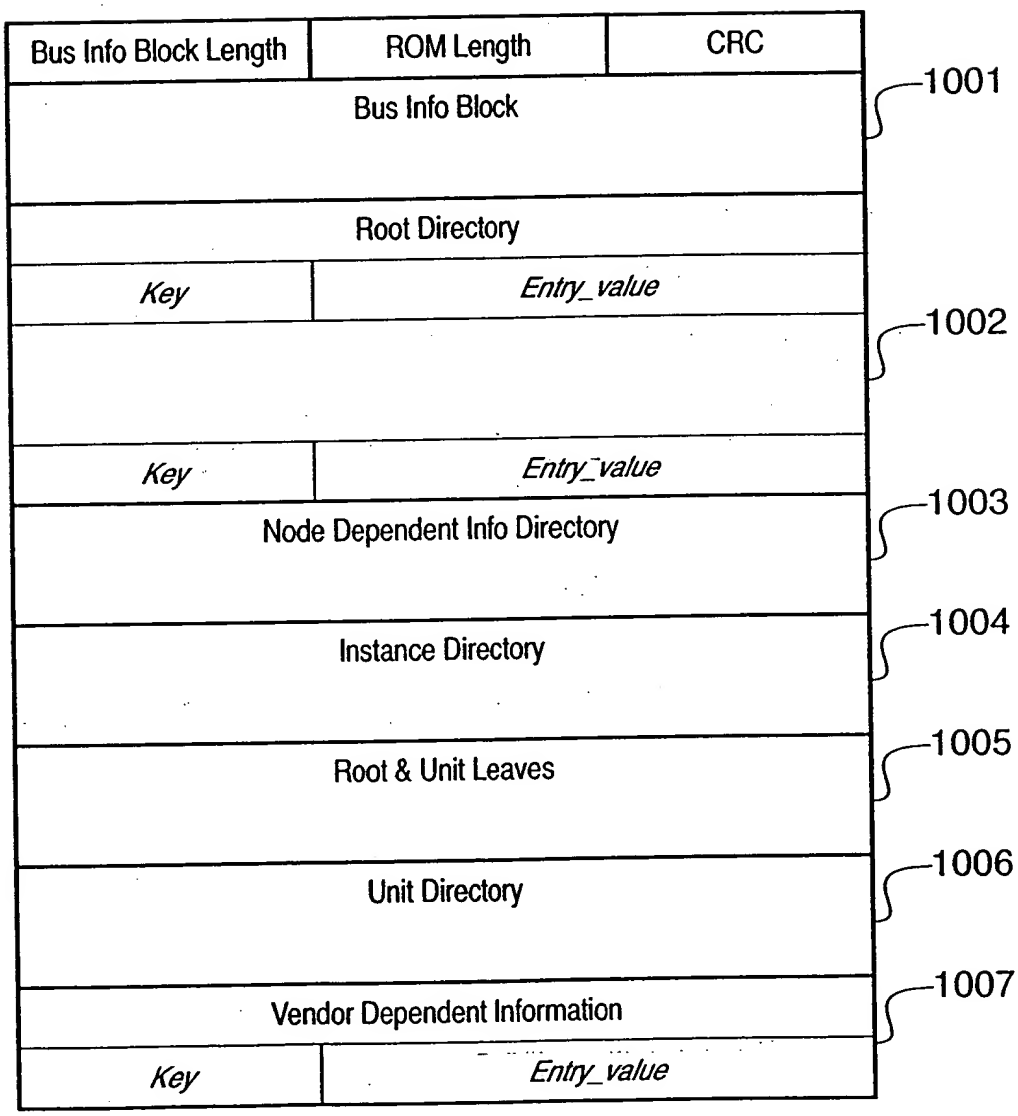

Bus Info Block Length
ROM Length
CRC
Bus Info Block
1001
Root Directory
Key
Entry_value
Key
Entry_value
1002
Node Dependent Info Directory
1003
Instance Directory
1004
Root & Unit Leaves
1005
Unit Directory
1006
Vendor Dependent Information
Key
Entry_value
1007

FIG. 10

| SERIAL BUS DEVICE REGISTER | | |
|---|---|---|
| OFFSET (HEXADECIMAL) | REGISTER NAME | FUNCTION |
| 800 ~ FFC | | RESERVATION |
| 1000 - ~ 13FC | TOPOLOGY_MAP | SERIAL BUS CONFIGURETION INFORMATION |
| 1400 ~ 1FFC | | RESERVATION |
| 2000 ~ 2FFC | SPEED_MAP | SERIAL BUS TRANSFER RATE INFORMATION |
| 3000 ~ FFFC | | RESERVATION |

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# FIG. 11

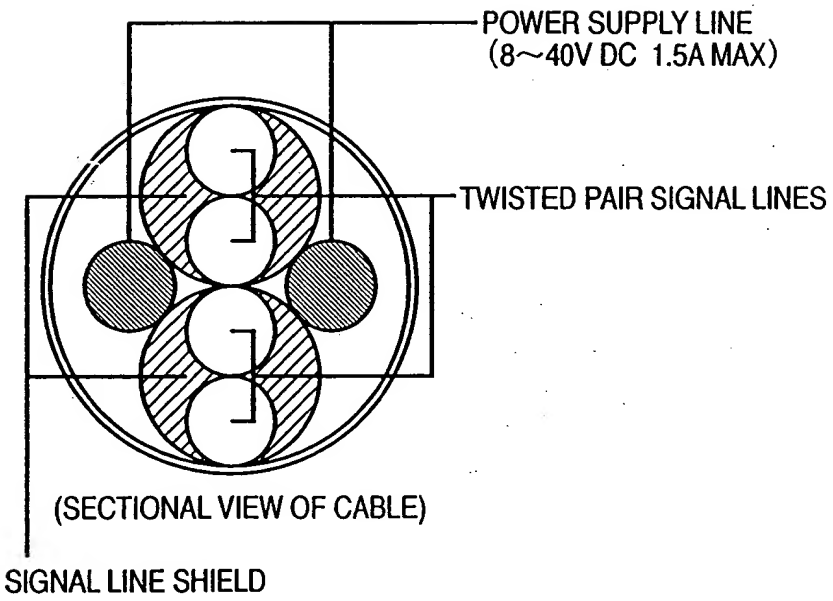


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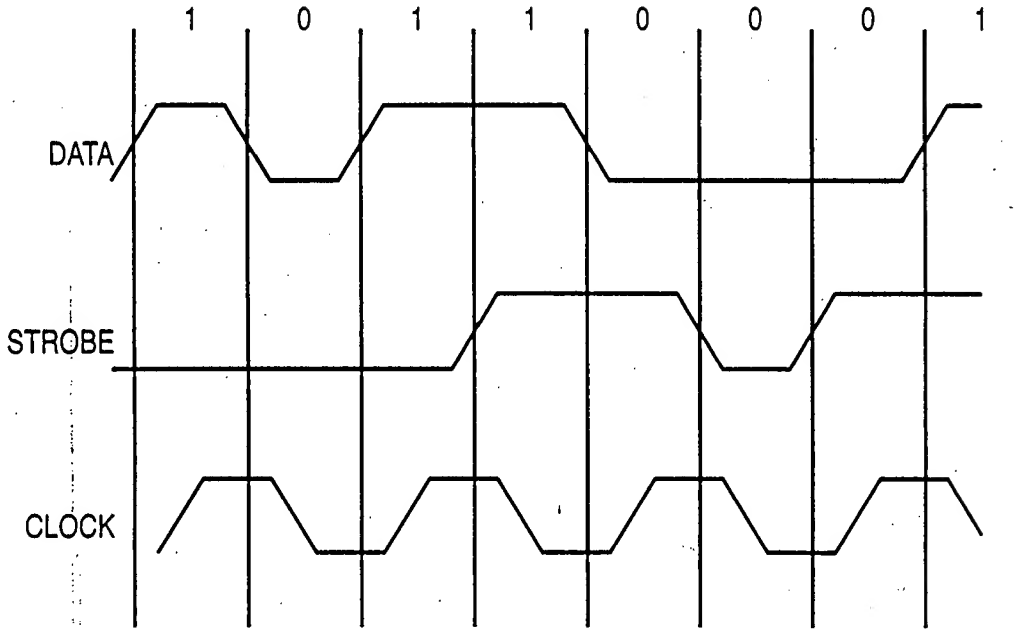
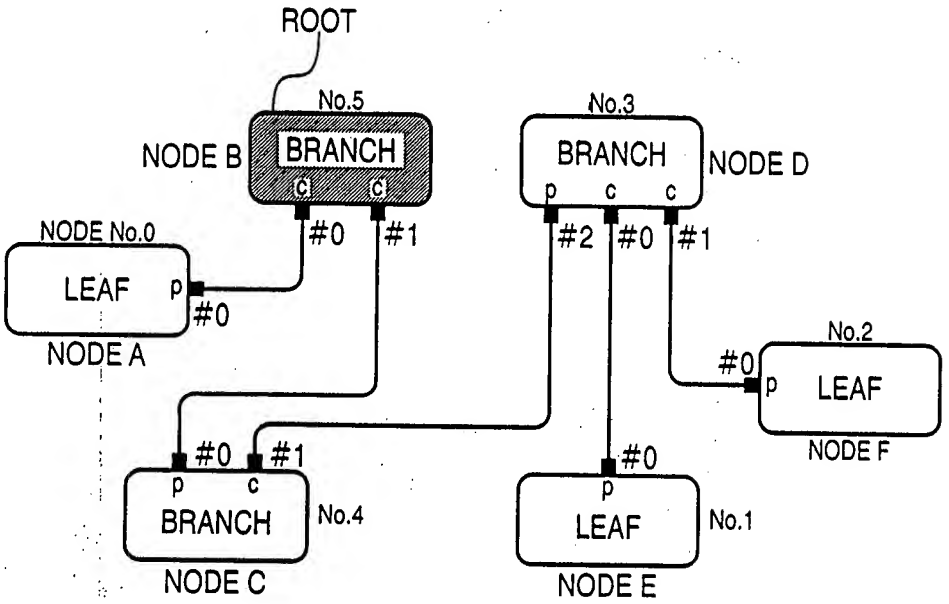
FIG. 12



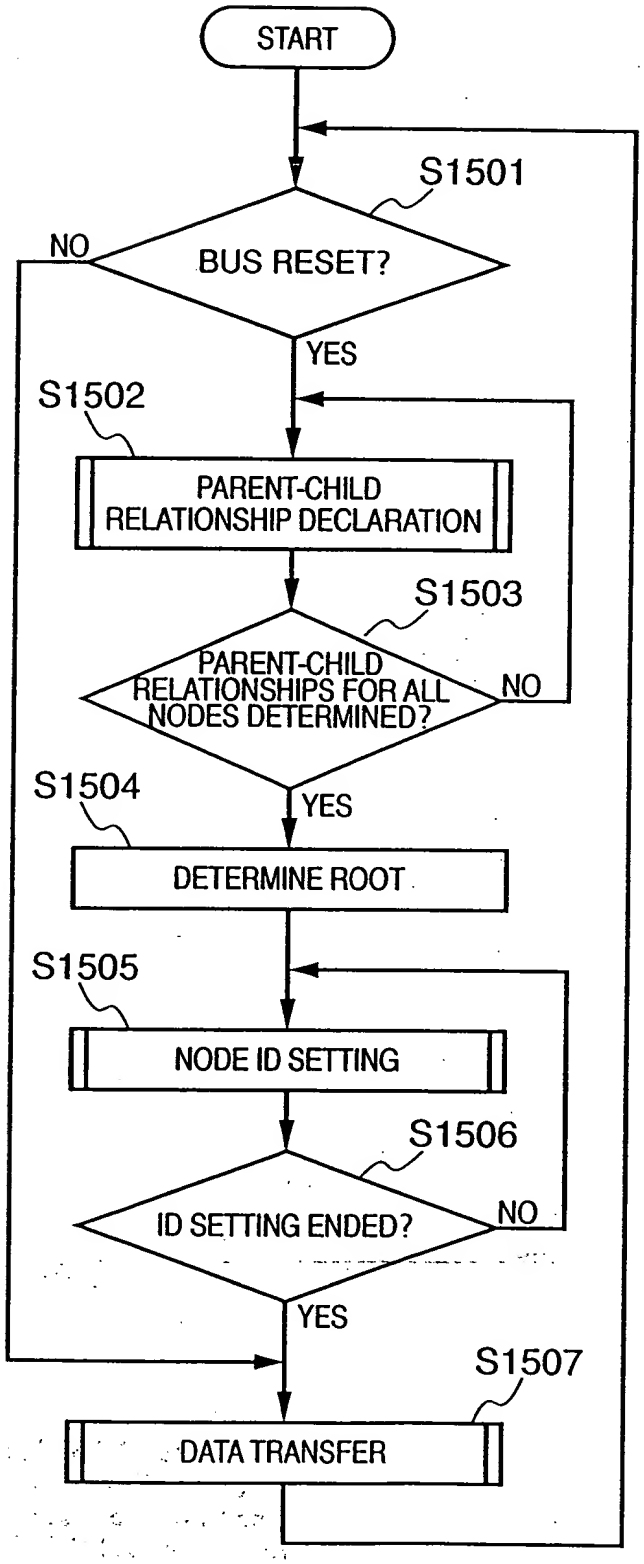

(CLOCK IS OBTAINED BY PERFORMING EXCLUSIVE OR DATA AND STROBE)

# FIG. 13




PORT
p :PARENT PORT CONNECTED TO PARENT NODE
c :CHILD PORT CONNECTED TO CHILD NODE

FIG. 14


START
S1501
BUS RESET?
NO
YES
S1502
PARENT-CHILD RELATIONSHIP DECLARATION
S1503
PARENT-CHILD RELATIONSHIPS FOR ALL NODES DETERMINED?
NO
YES
S1504
DETERMINE ROOT
S1505
NODE ID SETTING
S1506
ID SETTING ENDED?
NO
YES
S1507
DATA TRANSFER

# FIG. 15

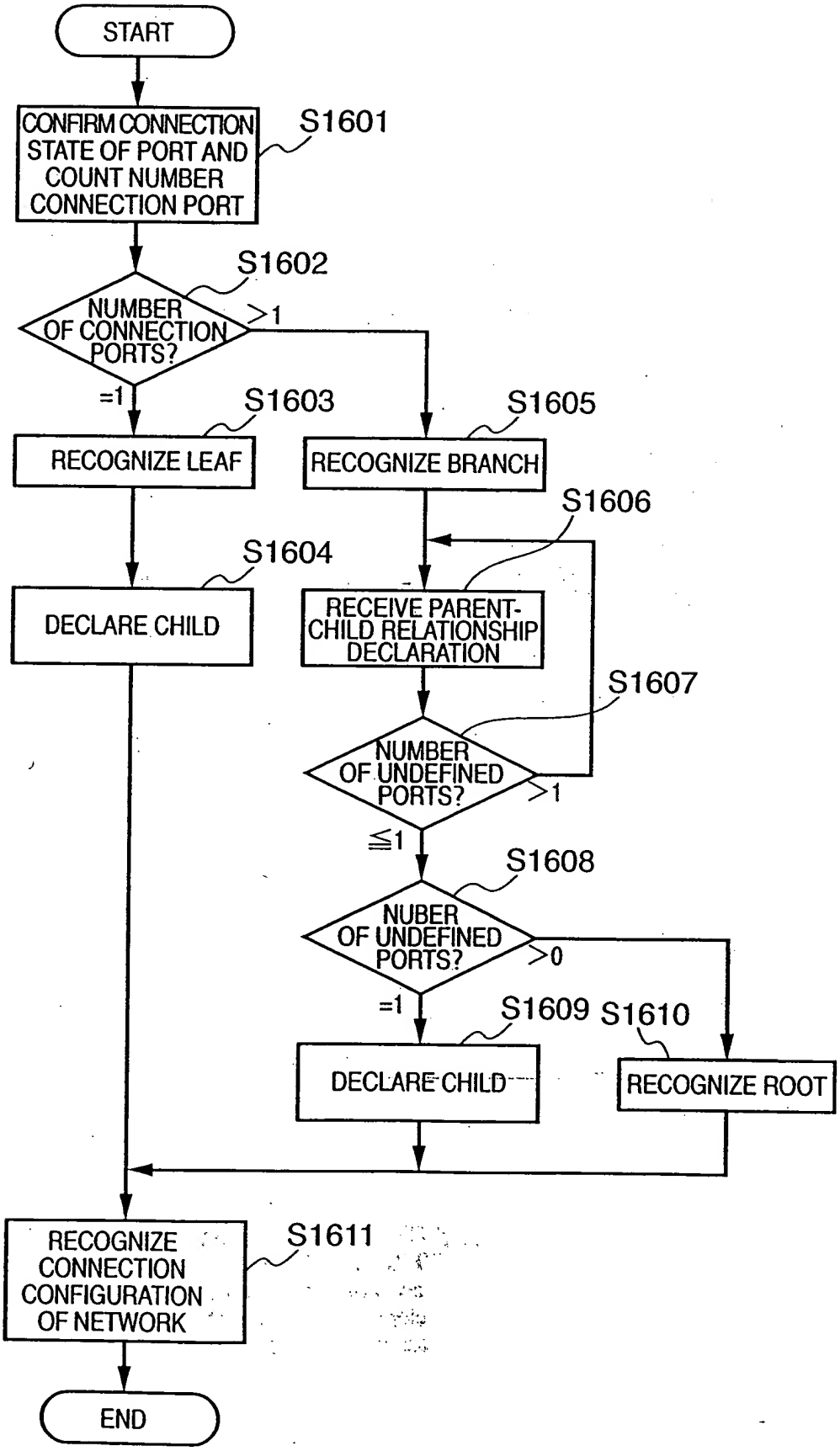

START
CONFIRM CONNECTION STATE OF PORT AND COUNT NUMBER CONNECTION PORT
S1601
S1602
NUMBER OF CONNECTION PORTS?
>1
=1
S1603
RECOGNIZE LEAF
S1605
RECOGNIZE BRANCH
S1606
S1604
DECLARE CHILD
RECEIVE PARENT-CHILD RELATIONSHIP DECLARATION
S1607
NUMBER OF UNDEFINED PORTS?
>1
≦1
S1608
NUBER OF UNDEFINED PORTS?
>0
=1
S1609
S1610
DECLARE CHILD
RECOGNIZE ROOT
RECOGNIZE CONNECTION CONFIGURATION OF NETWORK
S1611
END

FIG. 16

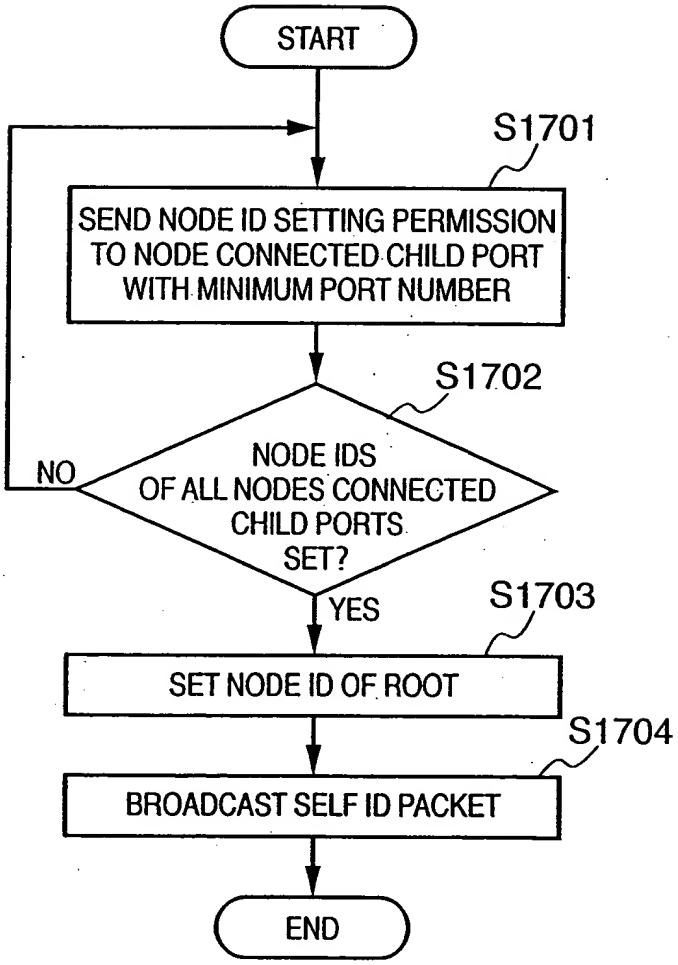

START
S1701
SEND NODE ID SETTING PERMISSION TO NODE CONNECTED CHILD PORT WITH MINIMUM PORT NUMBER
S1702
NODE IDS OF ALL NODES CONNECTED CHILD PORTS SET?
NO
YES
S1703
SET NODE ID OF ROOT
S1704
BROADCAST SELF ID PACKET
END

FIG. 17

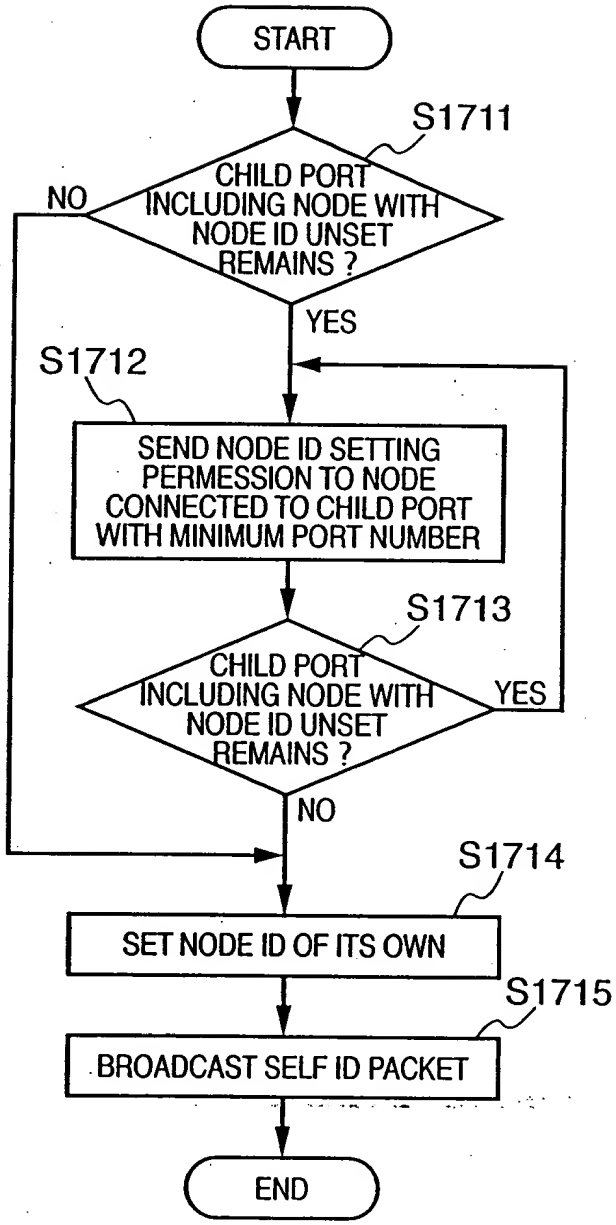

START
S1711
CHILD PORT INCLUDING NODE WITH NODE ID UNSET REMAINS ?
NO
YES
S1712
SEND NODE ID SETTING PERMESSION TO NODE CONNECTED TO CHILD PORT WITH MINIMUM PORT NUMBER
S1713
CHILD PORT INCLUDING NODE WITH NODE ID UNSET REMAINS ?
YES
NO
S1714
SET NODE ID OF ITS OWN
S1715
BROADCAST SELF ID PACKET
END

FIG. 18

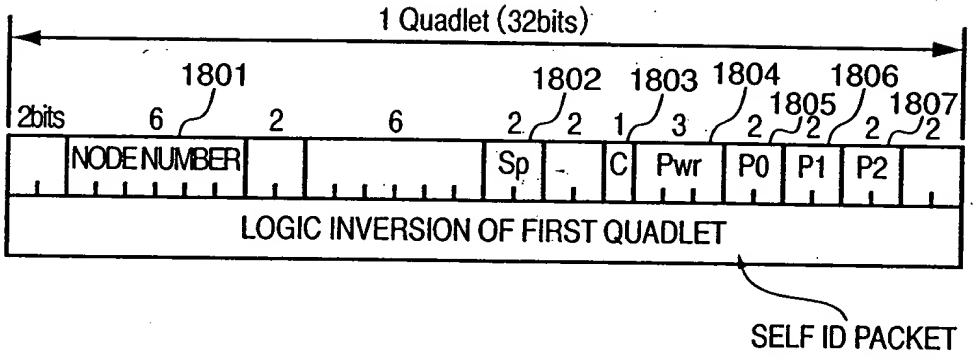
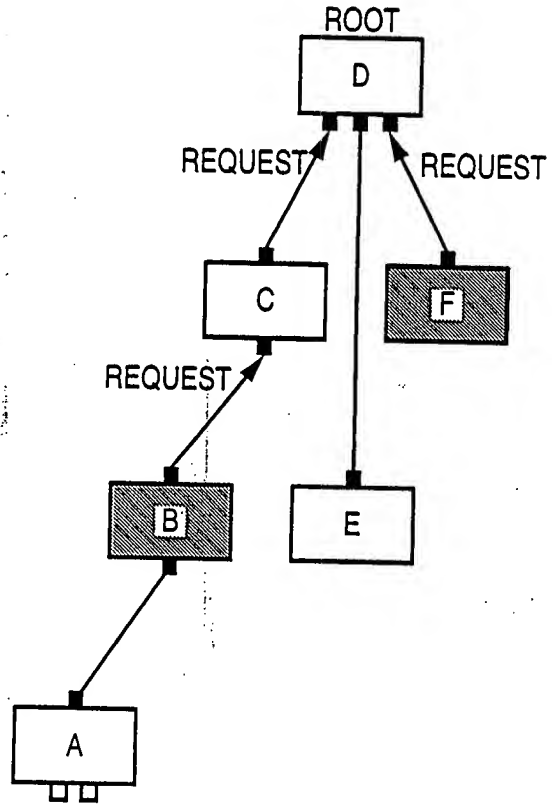
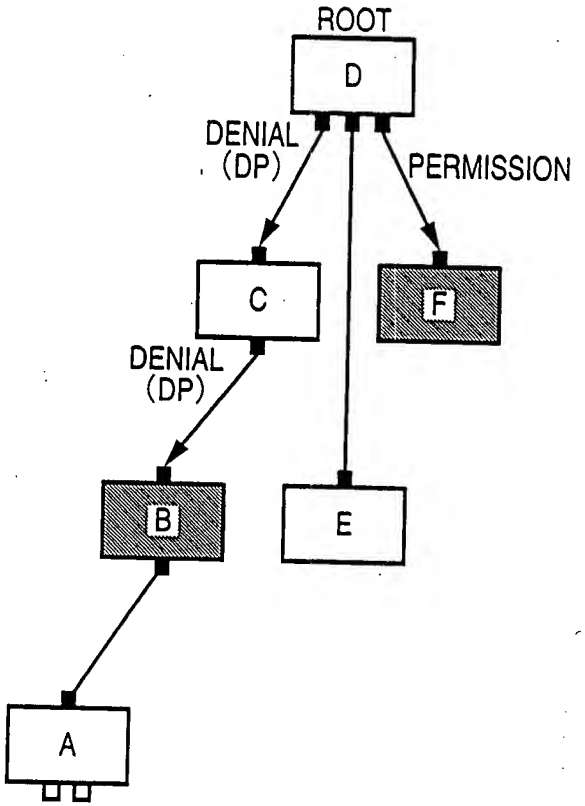

1 Quadlet (32bits)
1801
1802
1803
1804
1805
1806
1807
2bits
6
2
6
2
2
1
3
2
2
2
2
NODE NUMBER
Sp
C
Pwr
P0
P1
P2
LOGIC INVERSION OF FIRST QUADLET
SELF ID PACKET

FIG. 19A




BUS USE RIGHT REQUEST

FIG. 19B




PERMISSION/DENIAL OF BUS USE

FIG. 20

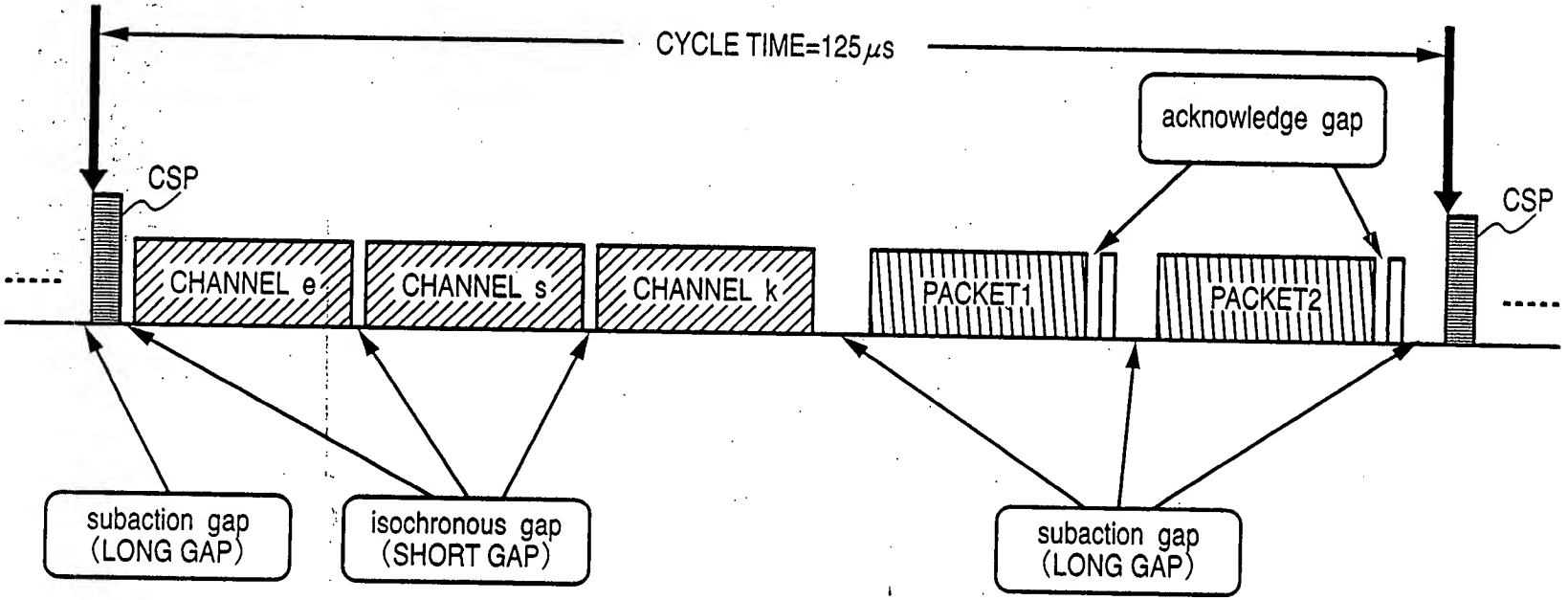

CYCLE TIME=125μs
acknowledge gap
CSP
CSP
CHANNEL e
CHANNEL s
CHANNEL k
PACKET1
PACKET2
subaction gap (LONG GAP)
isochronous gap (SHORT GAP)
subaction gap (LONG GAP)

FIG. 21

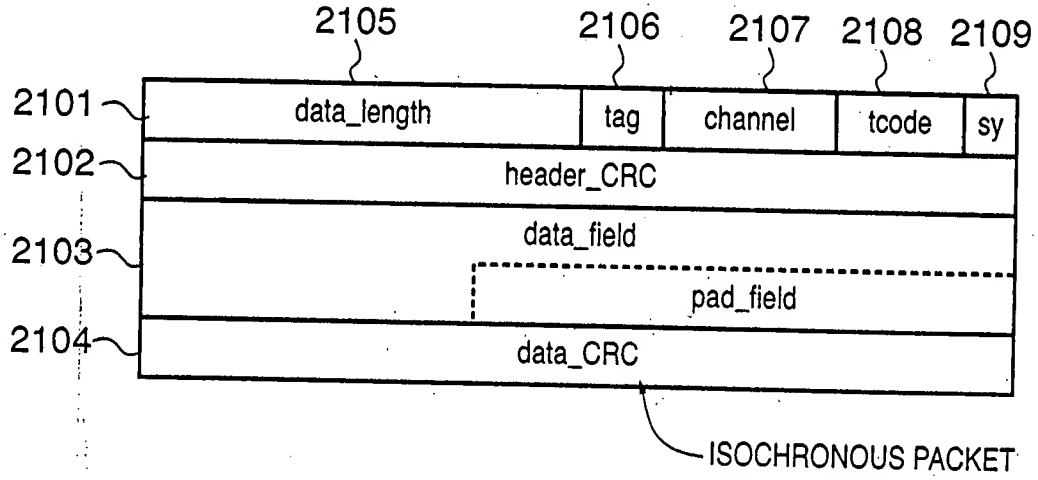

2105
2106
2107
2108
2109
2101
2102
2103
2104
data_length
tag
channel
tcode
sy
header_CRC
data_field
pad_field
data_CRC
ISOCHRONOUS PACKET

FIG. 22

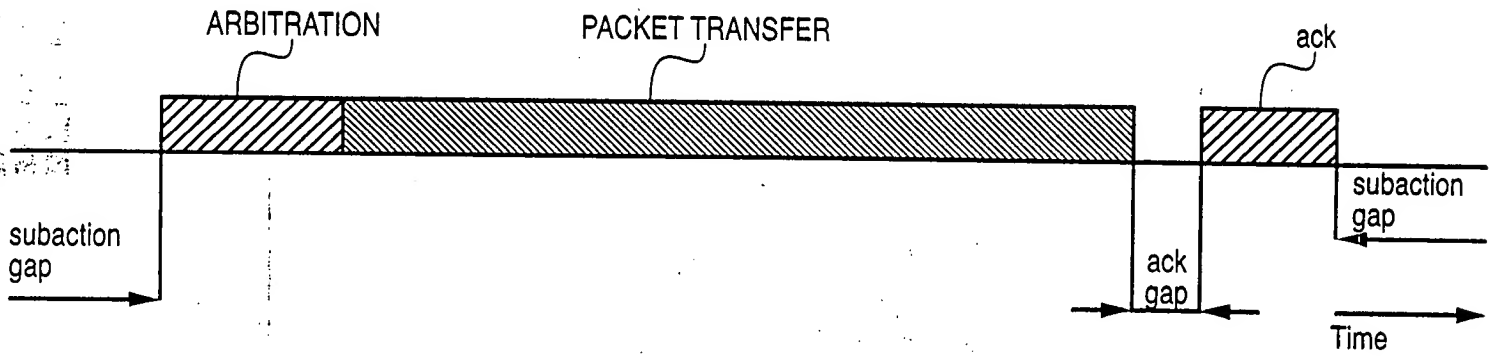
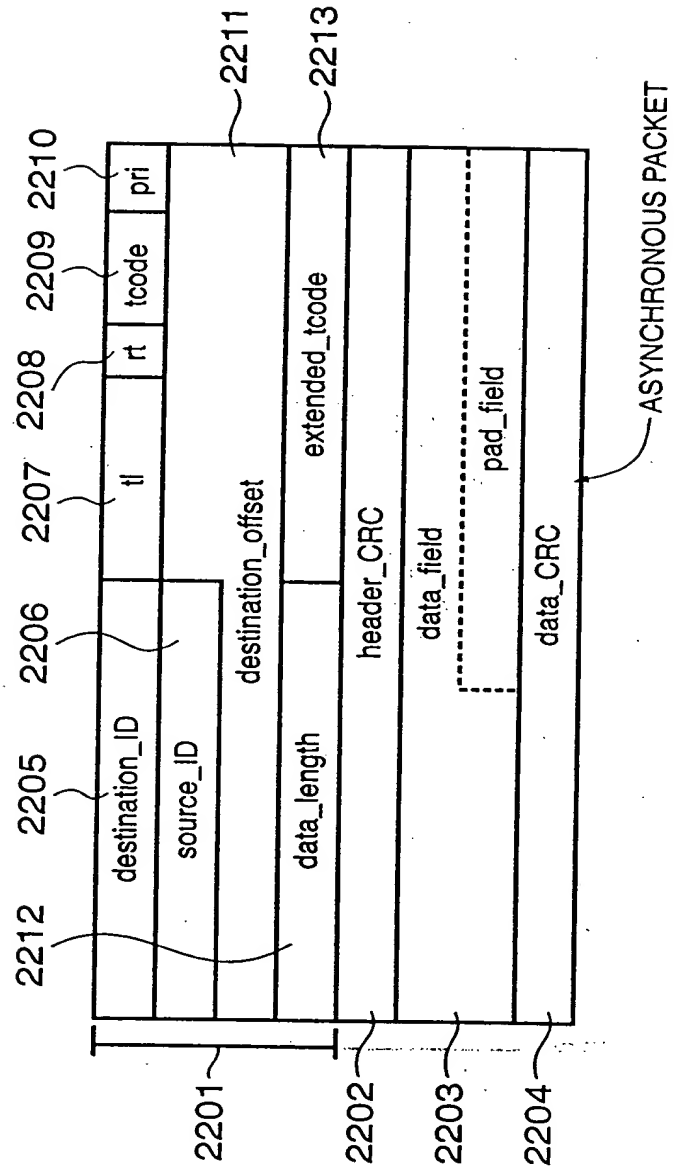

ARBITRATION
PACKET TRANSFER
ack
subaction gap
ack gap
subaction gap
Time

FIG. 23


2211
2213
2210
2209
2208
2207
2206
2205
2212
pri
tcode
rt
tl
destination_ID
source_ID
destination_offset
data_length
extended_tcode
header_CRC
data_field
pad_field
data_CRC
ASYNCHRONOUS PACKET
2201
2202
2203
2204

# FIG. 24

| ABBREVIATION | NAME | CONTENTS |
|---|---|---|
| destination_ID | destination identifier | INDICATING ID OF DESTINATION NODE (ONLY FOR ASYNSHRONOUS) |
| tl | transaction label | LABEL THAT INDICATES SERIES OF TRANSACTION (ONLY FOR ASYNSHRONOUS) |
| rt | retry code | CODE THAT INDICATES RE-SEND STARUS (ONLY FOR ASYNCHRONOUS) |
| tcode | transaction code | CODE THAT INDICATES TYPE OF PACKET (ONLY FOR ASYNCHRONOUS) |
| prt | priority | PRIORITY ORDER (ONLY FOR ASYNCHRONOUS) |
| source_ID | source identifier | INDICATION ID OF SOURCE NODE (ONLY FOR ASYNCHRONOUS) |
| destination_ offset | destination memory address | MEMORY ADDRESS OF DESTINATION NODE (ONLY FOR ASYNCHRONOUS) |
| rcode | response code | RESPONSE STATUS (ONLY FOR ASYNCHRONOUS) |
| quadlet_data | quadlet (4bytes) data | 4-BYTE LONG DATA (ONLY FOR ASYNCHRONOUS) |
| data_length | length of data | LENGTH OF data_field (EXCEPT pad bytes) |
| extended_ tcode | extended transaction code | EXTENDED TRANSACTION CODE (ONLY FOR ASYNCHRONOUS) |
| channel | isochronous identifier | IDENTIFYING ISOCHRONOUS PACKET |
| sy | synchronization code | USED TO SYNCHRONIZE VIDEO AND AUDIO (ONLY FOR ISOCHRONOUS) |
| cycle_time_ data | contents of the CYCLE_TIME register | VALUE OF CYCLE TIMER REGISTER OF CYCLE MASTER NODE (ONLY FOR CYCLE PACKET) |
| data_field | data +pad bytes | STORING DATA (ISOCHRONOUS AND ASYNCHRONOUS) |
| header_CRC | CRC for header field | CRC FOR HEADER FIELD |
| data_CRC | CRC for data field | CRC FOR DATA FIELD |
| tag | tag label | LABEL INDICATING FORMAT OF ISOCHRONOUS PACKET |

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FIG. 25

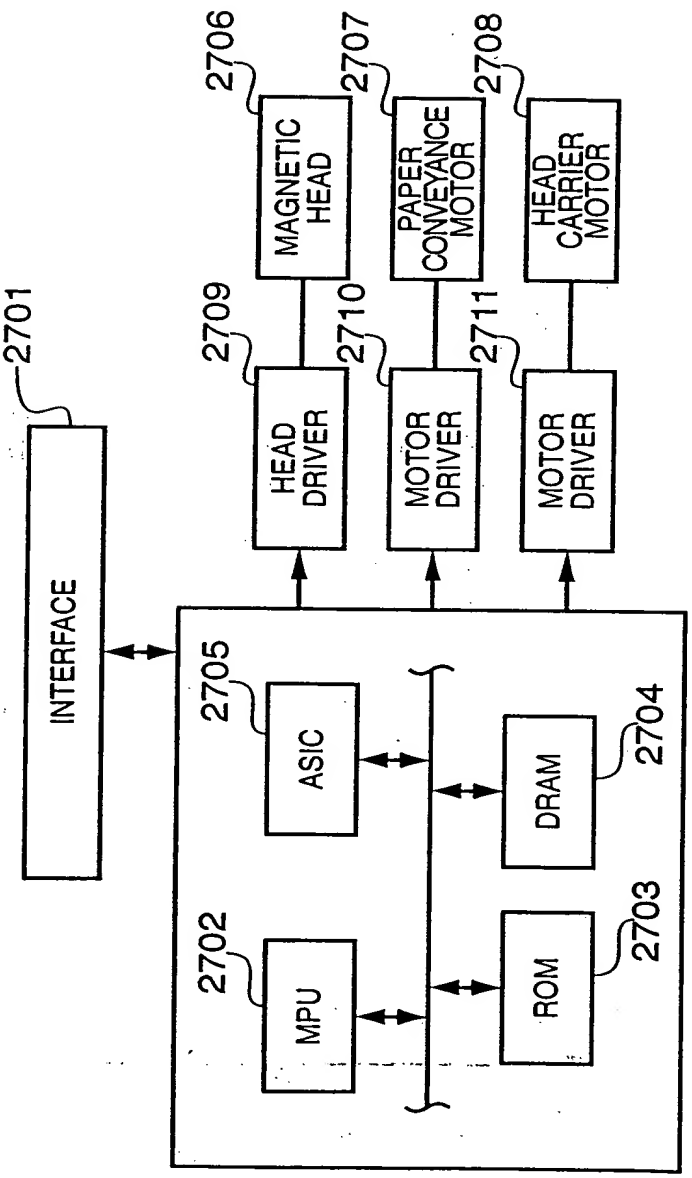
2701
INTERFACE
2705
ASIC
2702
MPU
2704
DRAM
2703
ROM
2709
HEAD DRIVER
2710
MOTOR DRIVER
2711
MOTOR DRIVER
2706
MAGNETIC HEAD
2707
PAPER CONVEYANCE MOTOR
2708
HEAD CARRIER MOTOR

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FIG. 26

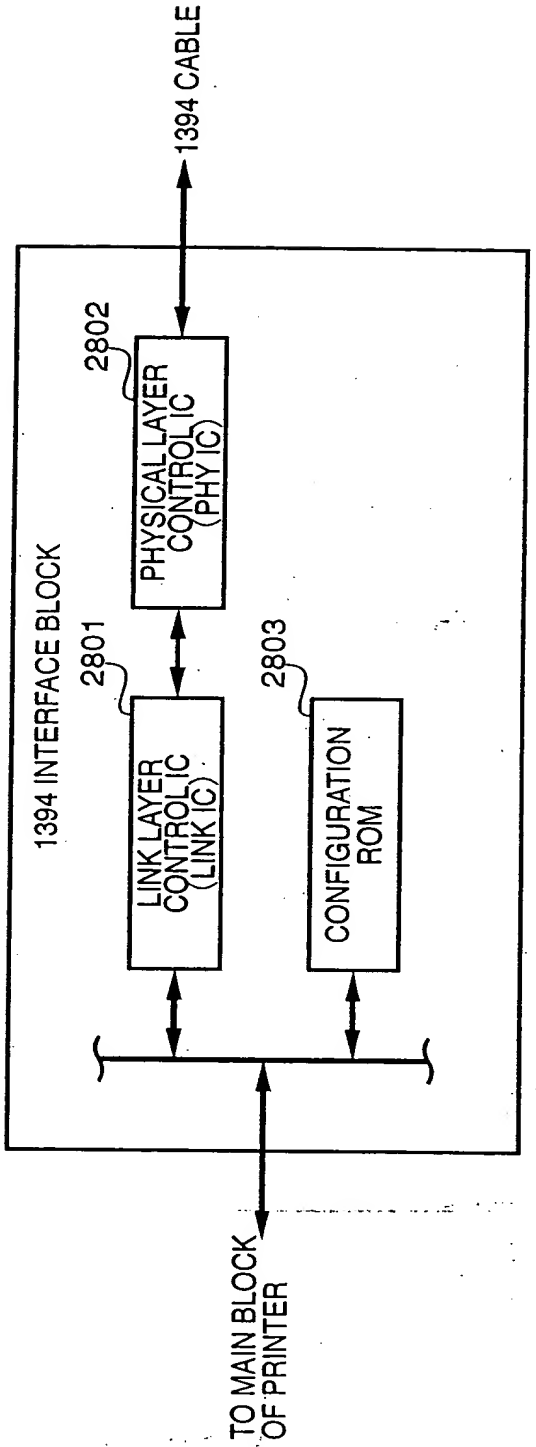
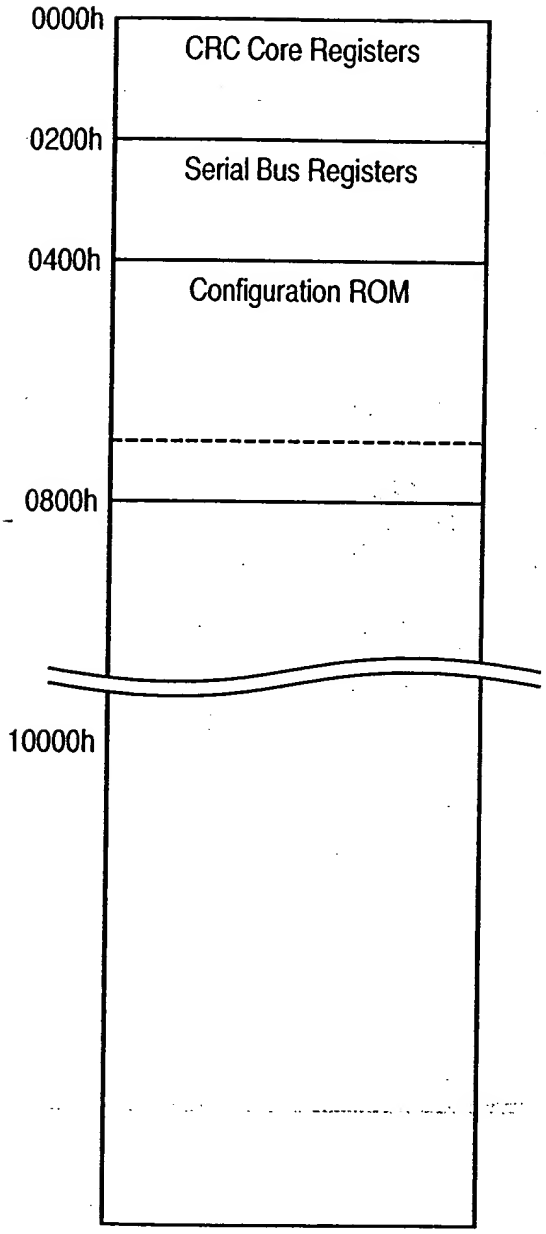


FIG. 27

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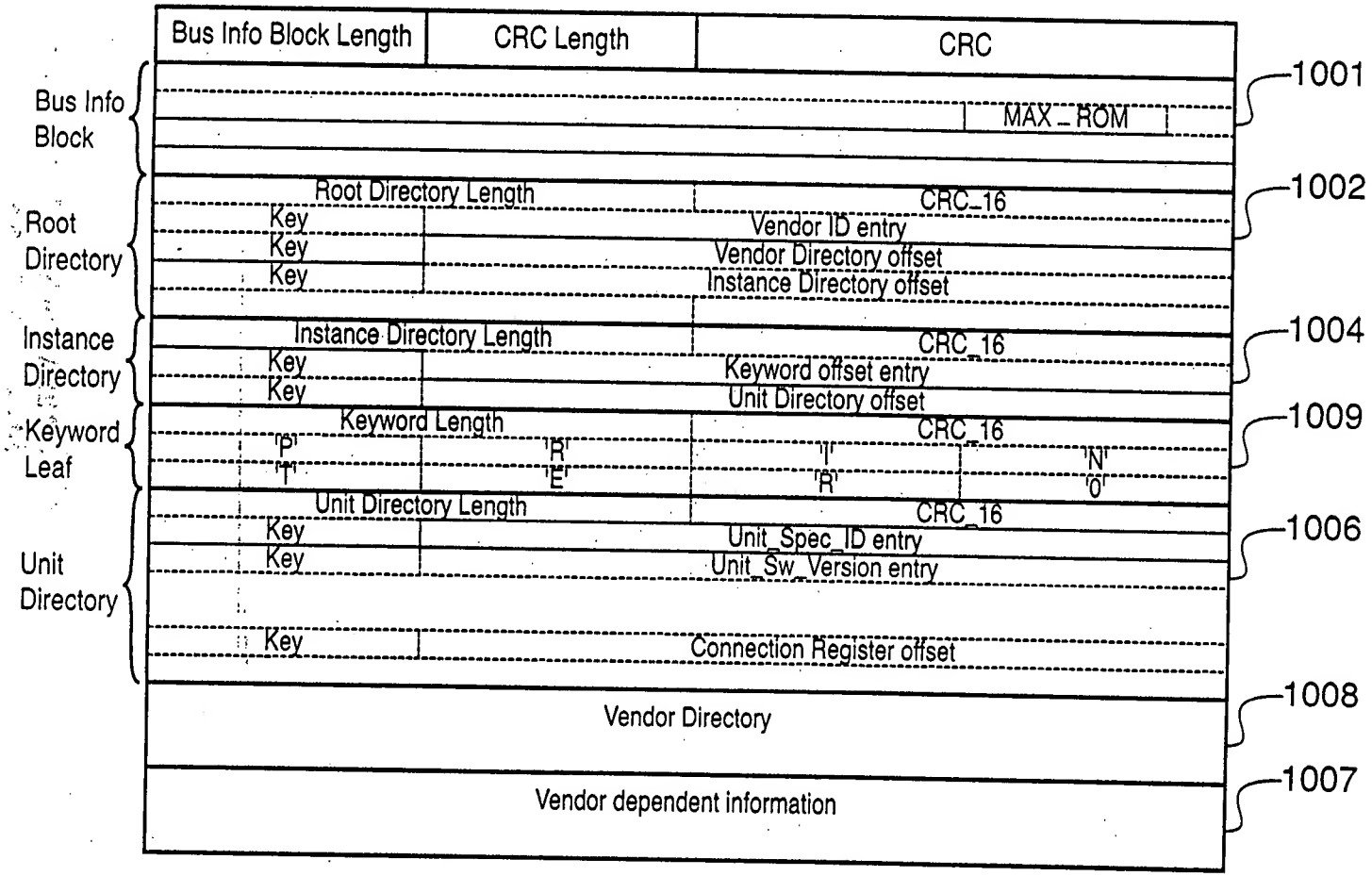
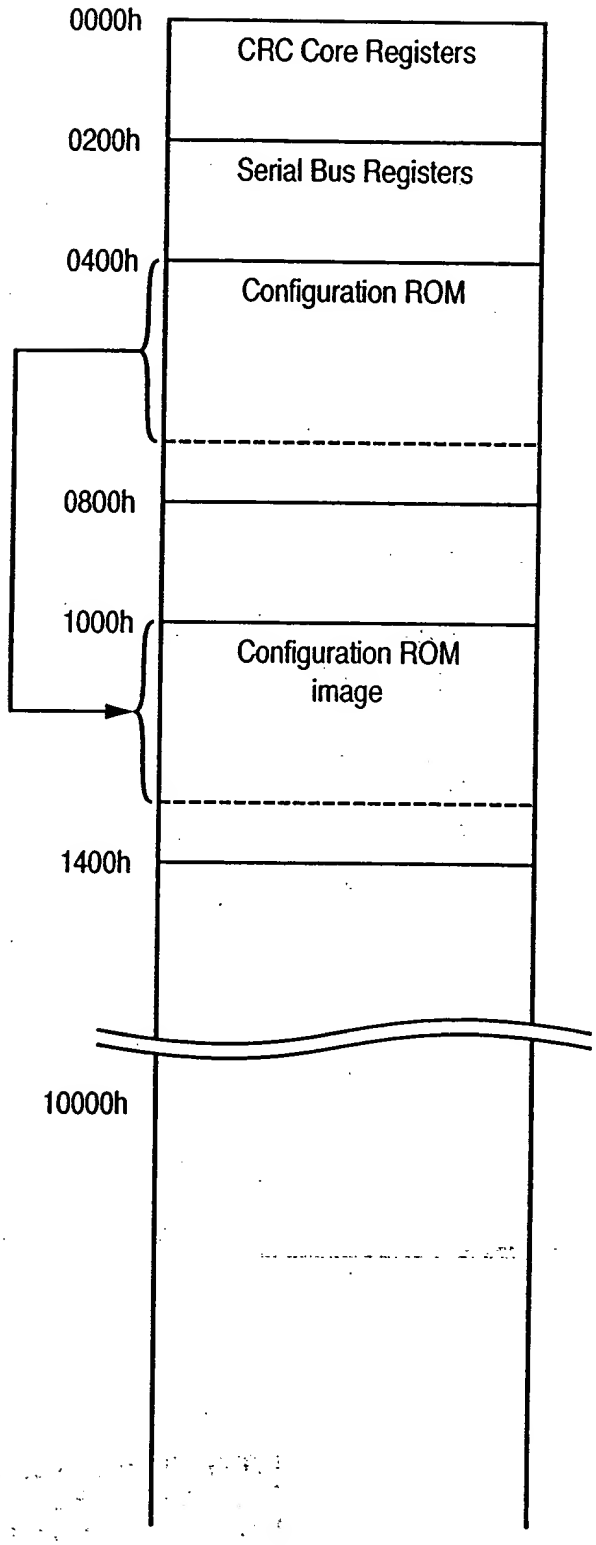
# FIG. 28

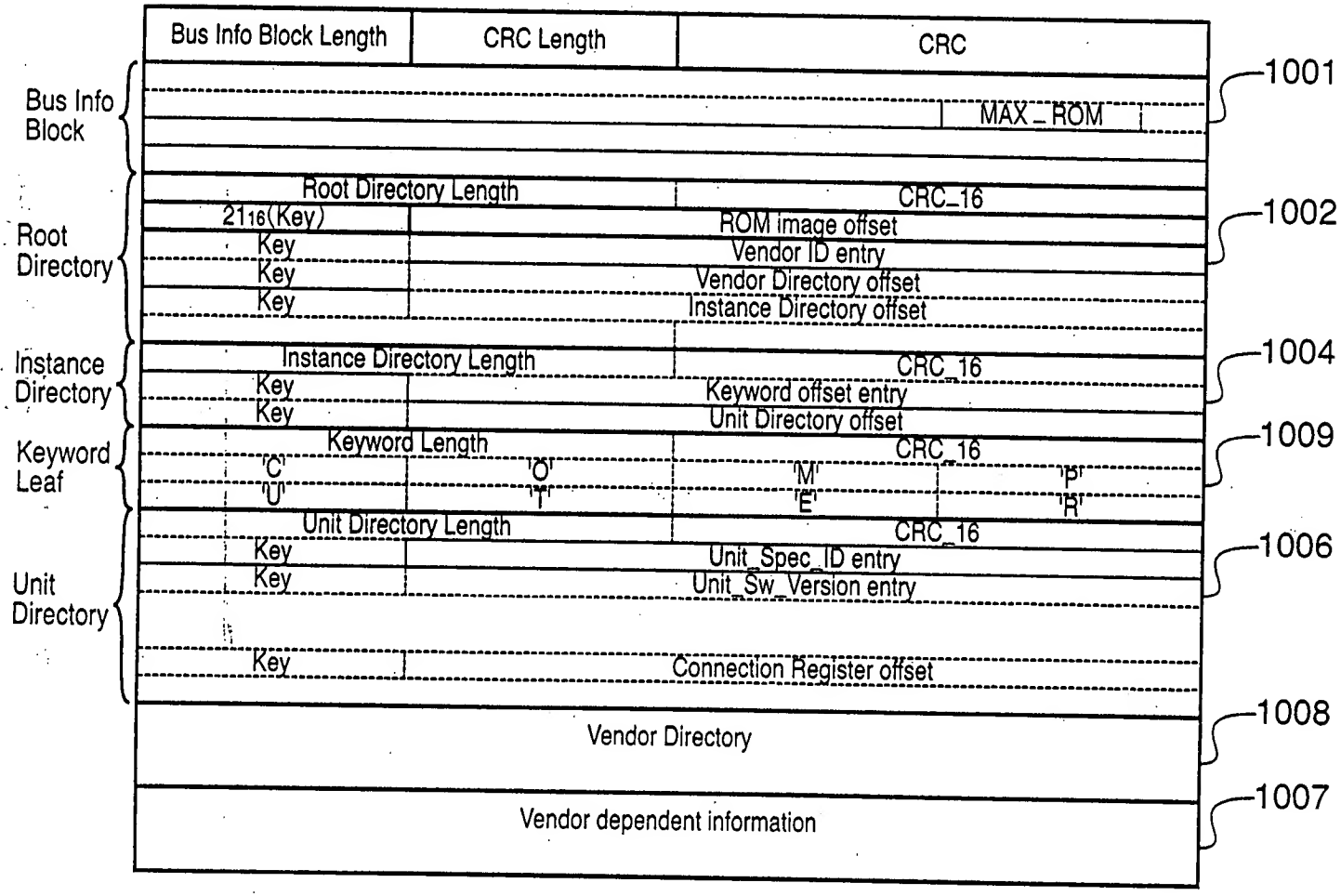

Bus Info Block Length
CRC Length
CRC
Bus Info Block
MAX_ROM
1001
Root Directory
Root Directory Length
CRC_16
Key
Vendor ID entry
Key
Vendor Directory offset
Key
Instance Directory offset
1002
Instance Directory
Instance Directory Length
CRC_16
Key
Keyword offset entry
Key
Unit Directory offset
1004
Keyword Leaf
Keyword Length
CRC_16
'P' 'R' 'I' 'N'
'T' 'E' 'R' '0'
1009
Unit Directory
Unit Directory Length
CRC_16
Key
Unit_Spec_ID entry
Key
Unit_Sw_Version entry
1006
Key
Connection Register offset
Vendor Directory
1008
Vendor dependent information
1007

# FIG. 29

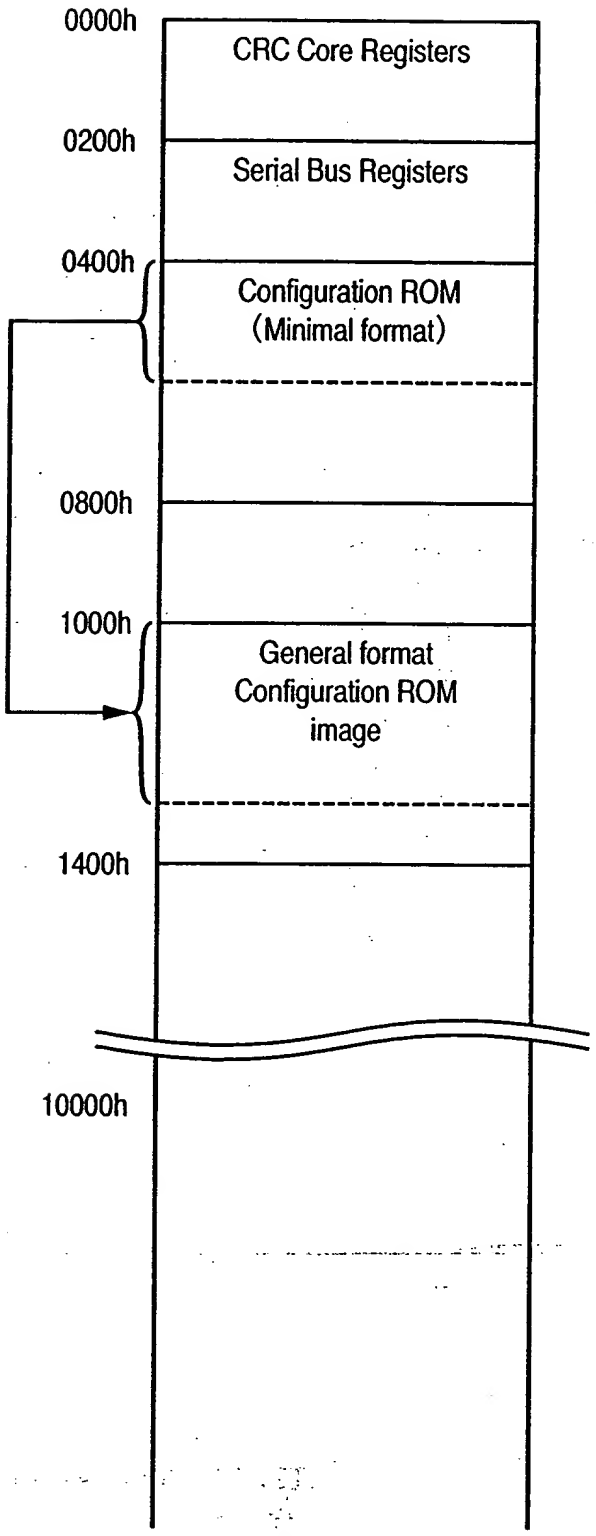



TOSHIBA - 0003960

# FIG. 30


Bus Info Block Length
CRC Length
CRC
MAX_ROM
Root Directory Length
CRC_16
21₁₆(Key)
ROM image offset
Key
Vendor ID entry
Key
Vendor Directory offset
Key
Instance Directory offset
Instance Directory Length
CRC_16
Key
Keyword offset entry
Key
Unit Directory offset
Keyword Length
CRC_16
'C'
'O'
'M'
'P'
'U'
'T'
'E'
'R'
Unit Directory Length
CRC_16
Key
Unit_Spec_ID entry
Key
Unit_Sw_Version entry
Key
Connection Register offset
Vendor Directory
Vendor dependent information
Bus Info Block
Root Directory
Instance Directory
Keyword Leaf
Unit Directory
1001
1002
1004
1009
1006
1008
1007

# FIG. 31


0000h
CRC Core Registers
0200h
Serial Bus Registers
0400h
Configuration ROM
(Minimal format)
0800h
1000h
General format
Configuration ROM
image
1400h
10000h

FUB280 9086E660

FIG. 32

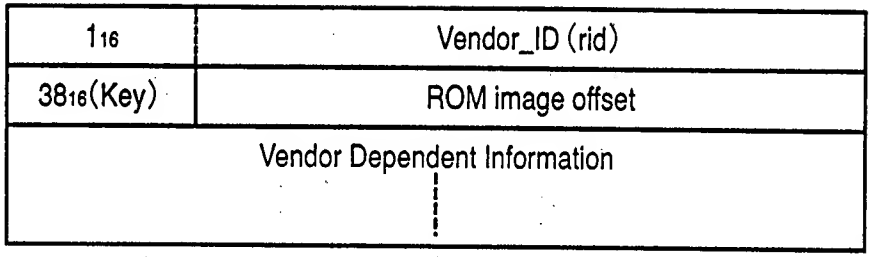
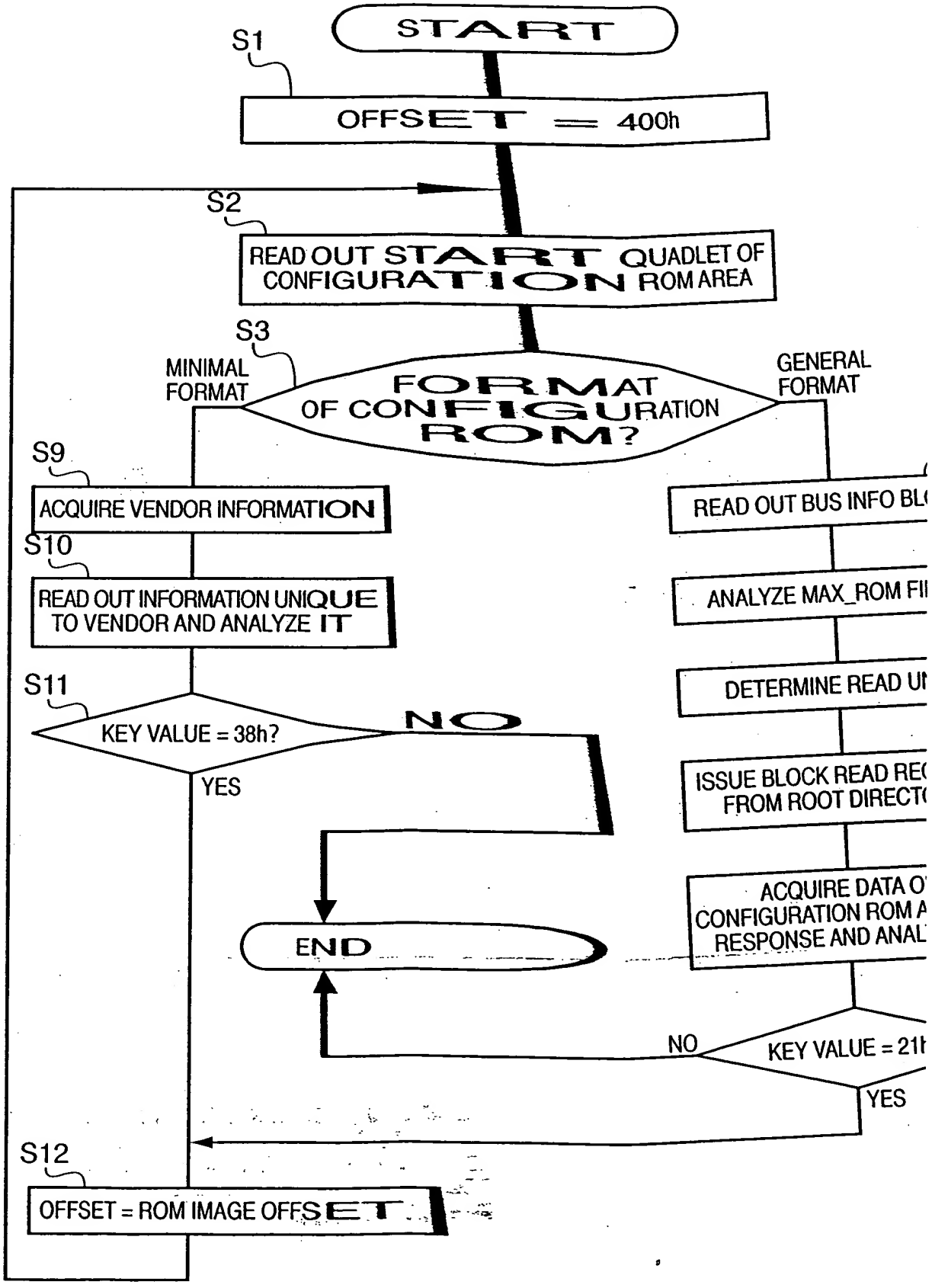
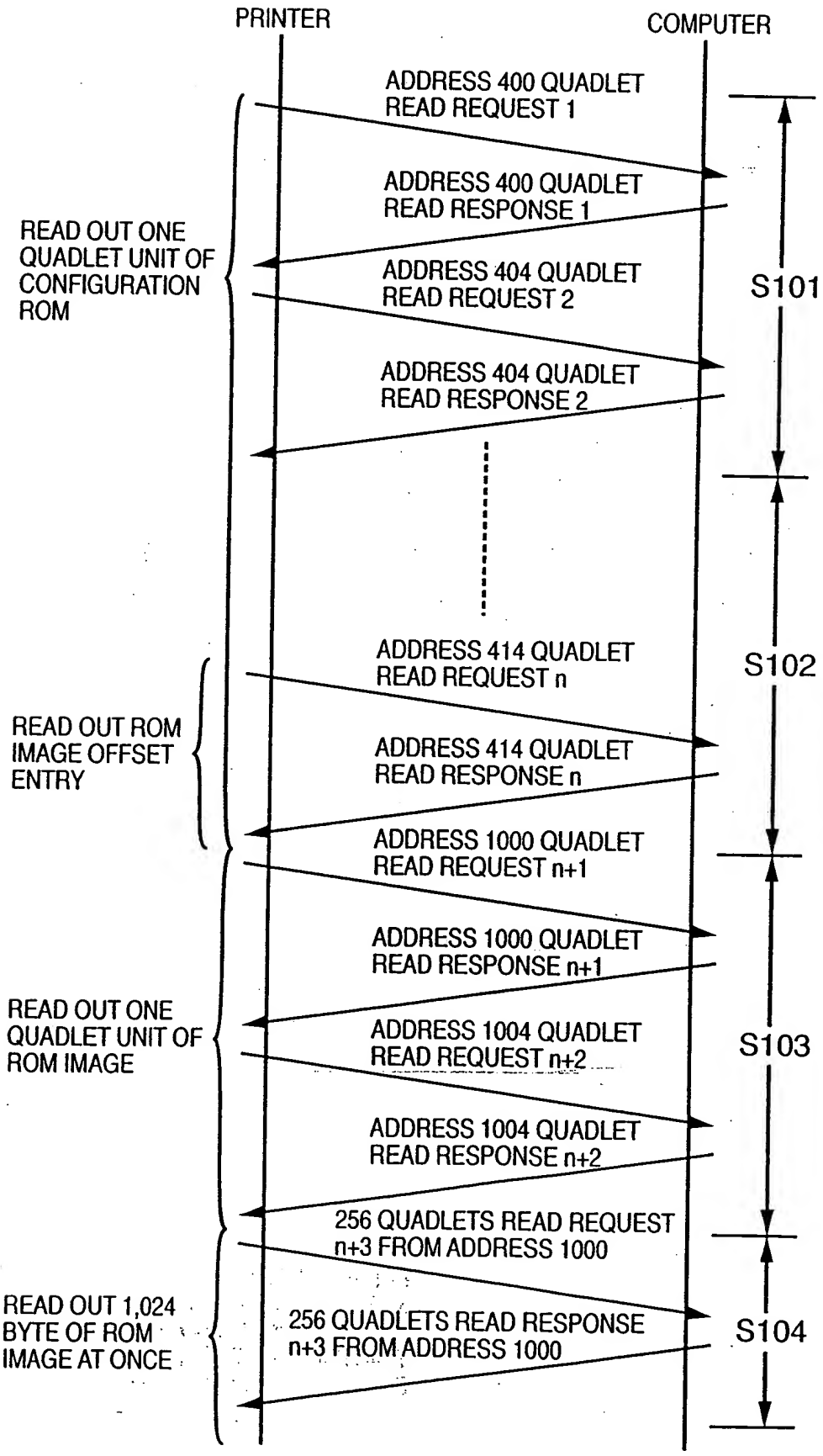


FIG. 33


START
S1
OFFSET = 400h
S2
READ OUT START QUADLET OF CONFIGURATION ROM AREA
S3
MINIMAL FORMAT
FORMAT OF CONFIGURATION ROM?
GENERAL FORMAT
S9
ACQUIRE VENDOR INFORMATION
S10
READ OUT INFORMATION UNIQUE TO VENDOR AND ANALYZE IT
S11
KEY VALUE = 38h?
NO
YES
END
S12
OFFSET = ROM IMAGE OFFSET
READ OUT BUS INFO BL
ANALYZE MAX_ROM FI
DETERMINE READ UI
ISSUE BLOCK READ REC FROM ROOT DIRECT
ACQUIRE DATA O CONFIGURATION ROM A RESPONSE AND ANAL
NO
KEY VALUE = 21h
YES

# FIG. 34


PRINTER
COMPUTER
ADDRESS 400 QUADLET READ REQUEST 1
ADDRESS 400 QUADLET READ RESPONSE 1
READ OUT ONE QUADLET UNIT OF CONFIGURATION ROM
ADDRESS 404 QUADLET READ REQUEST 2
ADDRESS 404 QUADLET READ RESPONSE 2
S101
ADDRESS 414 QUADLET READ REQUEST n
ADDRESS 414 QUADLET READ RESPONSE n
READ OUT ROM IMAGE OFFSET ENTRY
S102
ADDRESS 1000 QUADLET READ REQUEST n+1
ADDRESS 1000 QUADLET READ RESPONSE n+1
READ OUT ONE QUADLET UNIT OF ROM IMAGE
ADDRESS 1004 QUADLET READ REQUEST n+2
ADDRESS 1004 QUADLET READ RESPONSE n+2
S103
256 QUADLETS READ REQUEST n+3 FROM ADDRESS 1000
READ OUT 1,024 BYTE OF ROM IMAGE AT ONCE
256 QUADLETS READ RESPONSE n+3 FROM ADDRESS 1000
S104